Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT KRAFT and SCOTT H. PRENGLE

Appeal No. 2002-0321
Application No. 09/014,729

ON BRIEF

Before KIMLIN, WARREN and WALTZ, Administrative Patent Judges.

KIMLIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 10-17, all the claims remaining in the present application. Claim 10 is illustrative:

10. A method of fabricating an electronic device on a semiconductor substrate, said method comprising the steps of:

forming a gate insulator on said substrate, said gate insulator having a thickness;

forming a silicon-containing layer on said gate insulator, said siliconcontaining layer having a thickness;

forming a layer comprised of titanium and nitride on said siliconcontaining layer, said layer comprised of titanium and nitride having a thickness;

forming a layer comprised of tungsten on said layer comprised of titanium and nitride, said layer comprised of tungsten having a thickness;

forming a layer comprised of silicon and nitride on said layer comprised of tungsten, said layer comprised of silicon and nitride having a thickness;

patterning and selectively etching said layer comprised of silicon and nitride to expose a portion of said layer comprised of tungsten, said step of selectively etching of said layer comprised of silicon and nitride being selective against etching said layer comprised of tungsten;

selectively etching said exposed portion of said layer comprised of tungsten substantially simultaneously with etching a portion of said layer comprised of titanium and nitride so as to expose a portion of said silicon-containing layer, said step of selectively etching said exposed portion of said layer comprised of tungsten being selective against etching said layer of comprised of silicon and nitride; and

then, selectively etching said exposed portion of said silicon-containing layer so as to expose a portion of said gate insulator, said step of selectively etching said exposed portion of said silicon-containing layer being selectively against etching said layer comprised of titanium and nitride, said layer comprised of tungsten, and said layer comprised of silicon and nitride substantially unetched.

The examiner relies upon the following references as evidence of obviousness:

Wu	5,543,362	Aug. 06, 1996
Agnello	5,897,349	Apr. 27, 1999
Autryve	5,935,877	Aug. 10, 1999

Appellants' claimed invention is directed to a method of fabricating an electronic device on a semiconductor substrate. The method comprises forming the following consecutive layers on a gate insulator: (1) a silicon-containing layer, (2) a layer of titanium and nitride, (3) a tungsten layer, and (4) a silicon and nitride layer. Each of the layers are consecutively etched including, finally, the exposed portion of the silicon-containing layer. According to appellants, "[a]n advantage of the invention is providing a highly selective etch that allows for long overetches necessary for severe wafer topography" (page 2 of Brief, third paragraph).

Appealed claims 10-15 stand rejected under 35 U.S.C. § 103 as being unpatentable over Agnello in view of Wu. Claims 16 and 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over the stated combination of references further in view of Autryve.

We have thoroughly reviewed the respective positions advanced by appellants and the examiner. In so doing, it is our judgment that the examiner has failed to establish a prima facie case of obviousness for the claimed subject matter. Accordingly, for essentially those reasons expressed by appellants, we will not sustain the examiner's rejections.

The examiner acknowledges that Agnello, the primary reference, does not disclose the claimed step of "selectively etching the exposed portion of the polysilicon layer to expose a portion of the gate insulation layer after the step of selectively etching the tungsten layer" (page 4 of Answer, second paragraph). To remedy this deficiency the examiner cites Wu for its disclosure of selectively etching the exposed portion of a polysilicon layer in order to expose a portion of the gate oxide layer.

The flaw in the examiner's reasoning is, as urged by appellants, that there would have been no motivation for one of ordinary skill in the art to perform the claimed step of etching the silicon layer. This is so because "the polysilicon portion 9 is selectively etched prior to etching the metal and barriers 13 instead of after selectively etching the layer of tungsten as required by the claim" (page 4 of Brief, first paragraph, emphasis added). While we have no doubt that one of ordinary skill in the art could have performed the claimed steps in the order recited, this is not the standard for measuring obviousness under § 103. In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). The examiner has failed to set forth the requisite rationale underlying why one of ordinary skill in the

art would have been motivated to modify the process of Agnello in the manner claimed. If one of ordinary skill in the art would have appreciated an advantage in utilizing the claimed methodology rather than the one described in Agnello, this has not been divulged by the examiner.

The examiner's further reliance on Autryve in rejecting claims 16 and 17 does not remedy the basic deficiency of the combined teachings of Agnello and Wu outlined above.

In conclusion, based on the foregoing, the examiner's decision rejecting the appealed claims is reversed.

REVERSED

EDWARD C. KIMLIN Administrative Patent Judge	)	
CHARLES F. WARREN Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
THOMAS A. WALTZ Administrative Patent Judge	)	

ECK:clm

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